

### **Company Information**

- **Educational Institution**
- **Two epitaxial growth reactors, one vertical hot wall and one horizontal cold wall, capable of handling 2 inch diameter wafers**
- **Complete Device processing and simulation capability**

### **Area of Expertise**

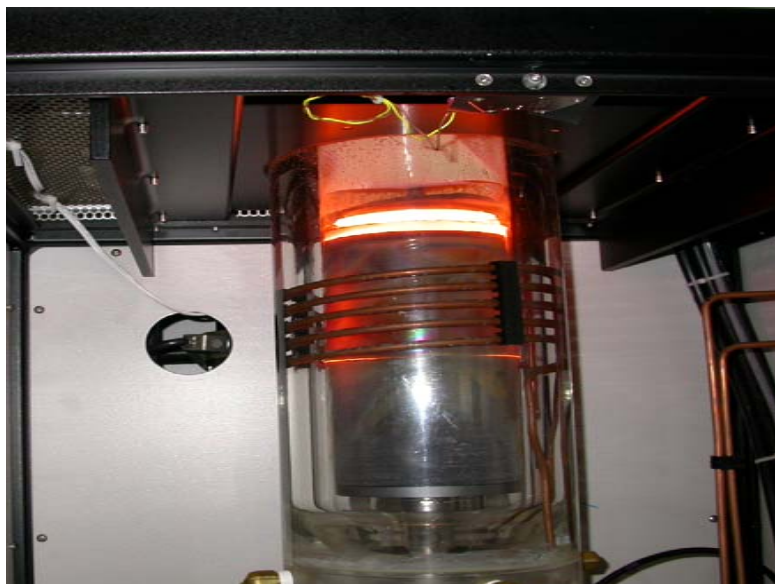
- **Epitaxial Growth of thick ( $>100\mu\text{m}$ ) 4H-SiC**
- **Continuous growth of epitaxial layers of p-on-n and n-on-p device structures**
- **Selective doping of SiC using selective epitaxial trench refill process**
- **Device processing (metallization, RIE etching and lithography)**
- **High temperature silane/argon annealing of ion implantation layers**

### **Previous Relevant Accomplishments**

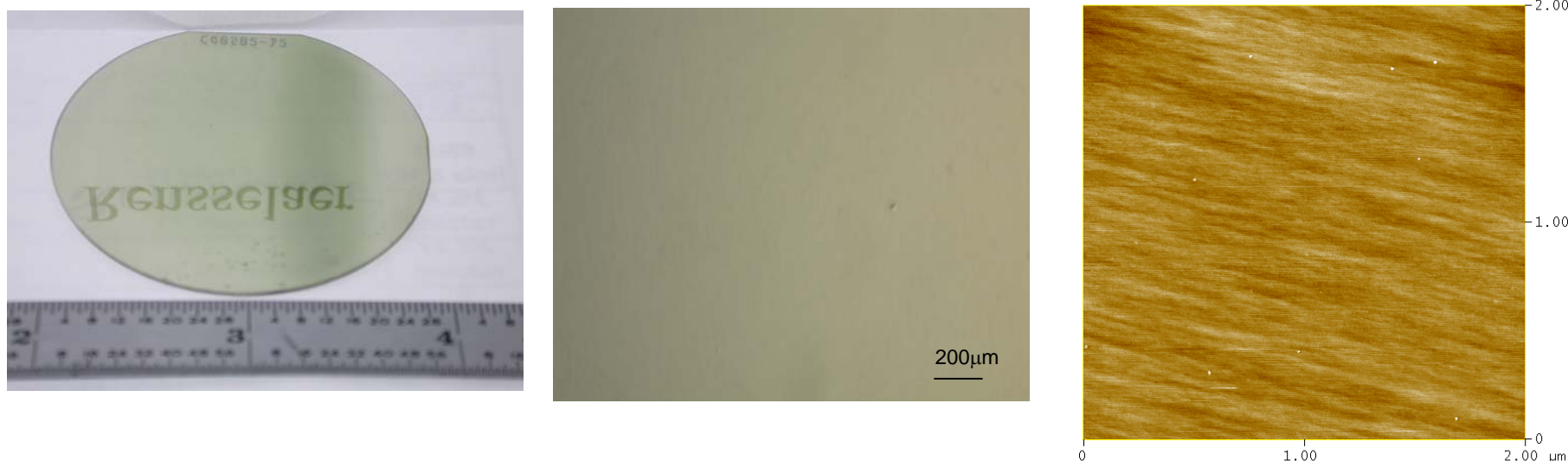
- **Demonstrated thick ( $>60\mu\text{m}$ ) epitaxial layers of 4H-SiC on 4H-SiC substrates with doping concentration less than  $2 \times 10^{14} \text{cm}^{-3}$ , and surface roughness less than 0.25nm over  $2\mu\text{m} \times 2\mu\text{m}$  area**
- **Demonstrated state of the art p-n junction devices on in-house grown layers**
- **Demonstrated selective growth process for trench refilling of partially processed wafers**
- **Wafer polishing process for damage-free material removal**

### **Contact Information**

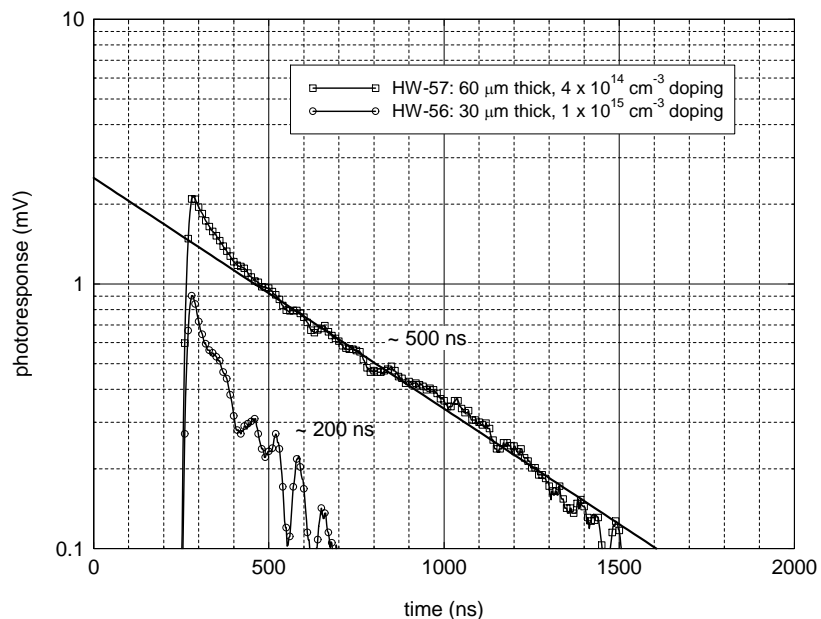
**Ishwara Bhat & T. Paul Chow**  
**ECSE Department**  
**Rensselaer Polytechnic Institute**  
**110 8<sup>th</sup> Street , JEC6003**  
**Troy, NY 12180-3590**  
**Phone: 518-276-2786; Fax: 518-276-6261**  
**Email: [bhati@rpi.edu](mailto:bhati@rpi.edu)**



**Figure 1 Vertical hot Wall reactor at RPI being used at 1630C. The reactor can handle two 2-inch diameter substrates. At right is the gas cabinet and the reactor chamber of horizontal SiC reactor.**



**Figure 2** A two inch diameter 60um thick SiC epitaxial film grown on 4H-SiC substrate with growth rate of 15um/hr. The figures above show the camera photograph, an optical microscope image and AFM image illustrating the excellent quality of the films. The AFM surface roughness was 0.21nm over a 2umx2um area. The background doping is less than  $5 \times 10^{14} \text{cm}^{-3}$ .

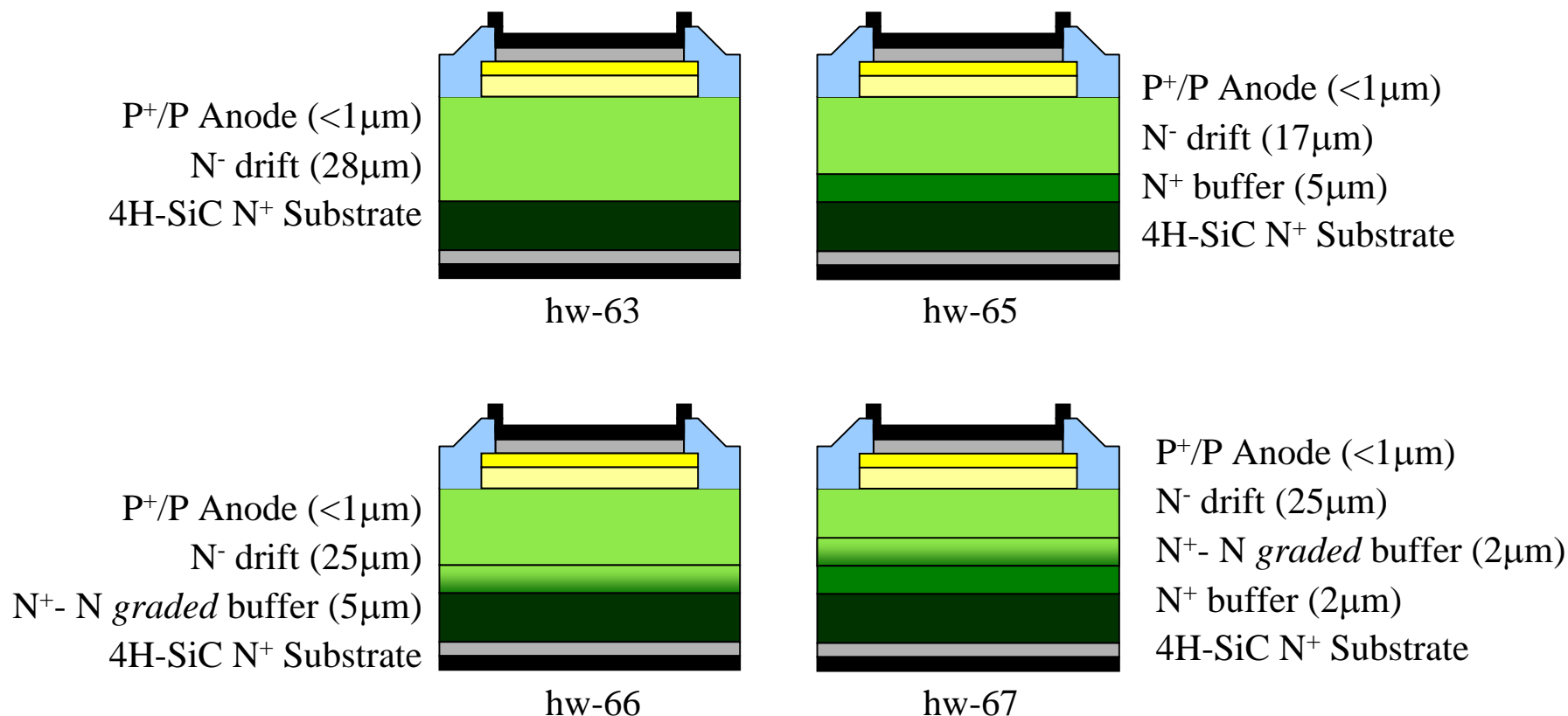


2" wafer, HW57B (61 $\mu\text{m}$ /4hours)	
Spot	Doping ( $\text{cm}^{-3}$ )
1	$3.2 \times 10^{14}$
2	$2.5 \times 10^{14}$
3	$4.6 \times 10^{14}$
4	$3.5 \times 10^{14}$
5	$4.5 \times 10^{14}$

Average  $\sim 500\text{ns}$  on  $60\mu\text{m}$  thick layer (HW57).

Doping variation over a 2-inch dia wafer

All epi-layers grown (*RPI*) on N<sup>+</sup> 4H-SiC substrates (*CREE*), and processed at RPI.

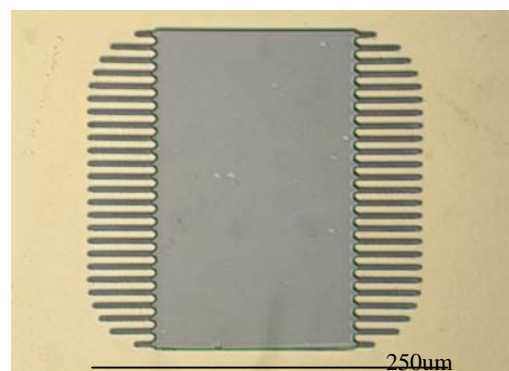
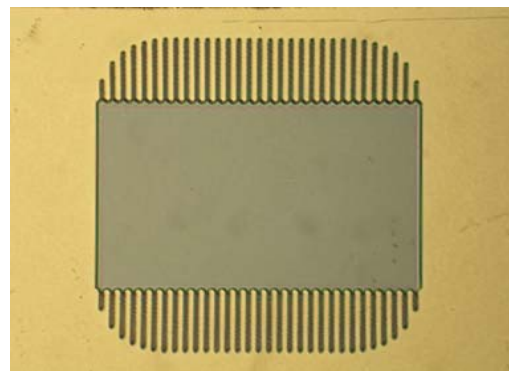
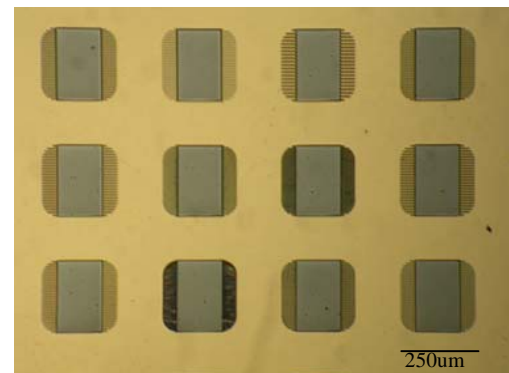
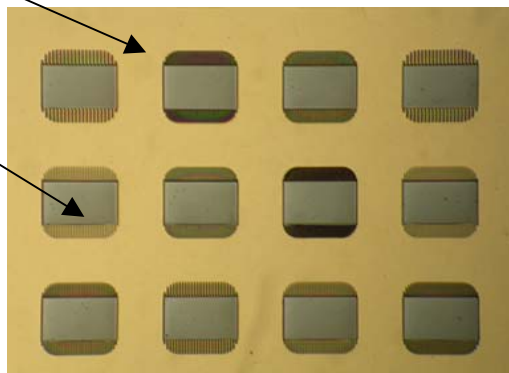


**Figure 3 Thick epi process for device fabrication.**  
EMC conference, June 2004

**Selective doping of SiC using selective growth.  
Less damage compared to ion implantation.**

Mask (no growth)

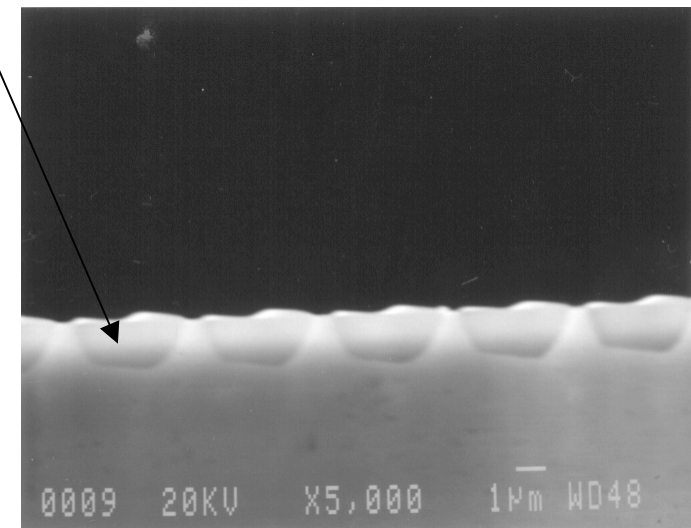
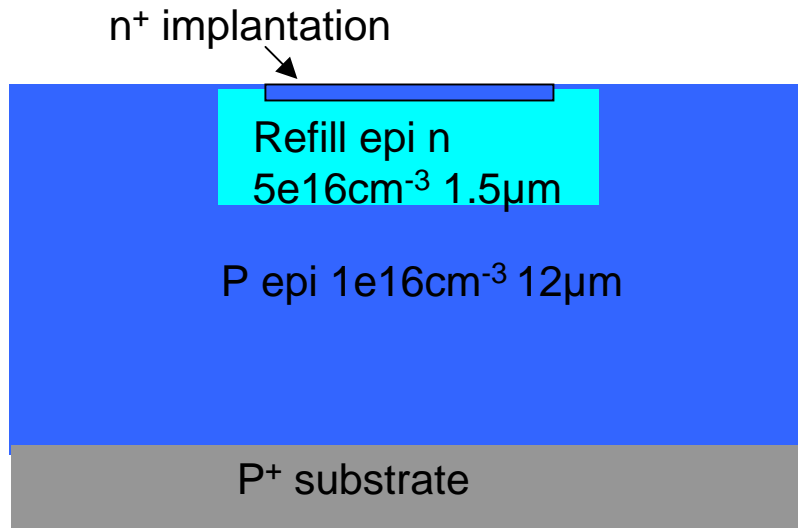
epi refill



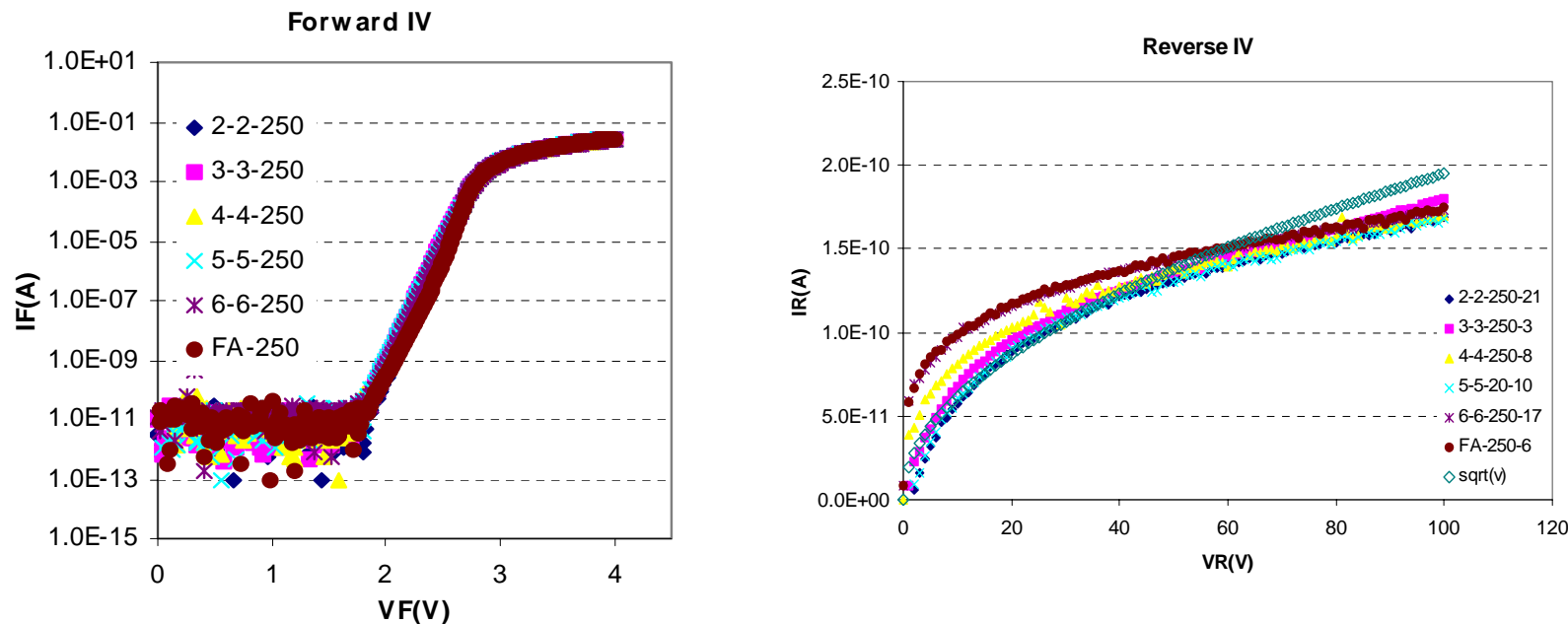
$\langle 11\bar{2}0 \rangle \longrightarrow$

$\langle 1\bar{1}00 \rangle \longrightarrow$

Refilled Square PN diode:  $L=250\mu\text{m}$  epi refill



$\langle 11\bar{2}0 \rangle \longrightarrow$



**Figure 4 I-V data of epi refilled pn junction diodes. Diodes of variable window width and mask width are used in the fabrication. For example, 2-2-250 indicates window width of  $2\mu\text{m}$ , masked width of  $2\mu\text{m}$  and overall area of  $250\mu\text{m} \times 250\mu\text{m}$ . FA-250 means no fingers (see figure 1). Diode area:  $6.2 \times 10^{-4} \text{ cm}^2$ . The I-V data are similar to the I-V data of mesa etched diodes.**